IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hisashi Ohtani et al.	Art Unit	: 2815
Serial No.	: 09/379,702	Examiner	: Eugene Lee
Filed	: August 24, 1999	Conf. No.	: 1613
Title	: METHOD OF FABRICATING SEMICONDUCTOR DEVICES		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, appellant responds to points raised for the first time in the Examiner's Answer of July 6, 2006 as follows.

In response to appellant's argument that a person of ordinary skill in the art would have been much more likely to take the first approach of replacing Yamazaki's thin gate insulating film with the two thicker films described by Matsumoto than the fourth approach of adding a second gate insulating film after the etching process illustrated by Yamazaki's Fig. 5C, the Examiner argues that the approach taken is not relevant since the claims are directed to an apparatus. However, this argument by the Examiner ignores the fact that the two approaches would produce different devices, and that the device produced by the first approach would not have satisfied the claim because neither film would have a side aligned with the side of the semiconductor island.

The Examiner then argues that the likelihood of choosing one approach over the other is based on appellant's speculation and that appellant has provided no factual evidence. Appellant agrees. However, appellant further asserts that the Examiner's conclusion about how the references would be combined is based on the Examiner's speculation and is not supported by factual evidence. Moreover, while appellant has provided a reasonable explanation as to why the first approach would have been chosen, the Examiner, who has the burden of showing how one of ordinary skill in the art would have been led to combine the references to reach the claimed subject matter, has provided no such explanation for choosing the fourth approach and, instead, has merely used a hindsight reconstruction of the invention to get to that position.

The Examiner then asserts that Matsumoto has provided a clear motivation to include an interlayer insulating film over Yamazaki's gate insulating film 3. Appellant disagrees and notes

that, as set forth in the Appeal Brief, Matsumoto, at best, provides a motivation for using a thicker gate insulating film. For the reasons that have already been presented, that motivation would not have led one of ordinary skill in the art to use the approach recited in the claims.

Finally, the Examiner asserts that the specification does not state that the side aligned with a side of the crystalline semiconductor island is critical to operation of the claimed device. Appellant respectfully asserts that the specification has no obligation to do so.

For these reasons, and the reasons stated in the Appeal Brief, appellant submits that the final rejection should be reversed.

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Respectfully submitted,

Barbara A. Benoit
Reg. No. 54,777

Date: Sept. 6, 2006

Barbara A Benoit for

John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331